What I claim is:

1. A semiconductor device, comprising:

a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

circuit patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the circuit pattern, formed in the dummy area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on an entire surface of the semiconductor substrate;

a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

2. A semiconductor device as claimed in claim 1, wherein the second insulating layer is a SOG layer.

3. A semiconductor device as claimed in claim 2, wherein the width of the first dummy pattern is fixed by a concentration of solid content of the SOG.

4. A semiconductor device as claimed in claim 1, wherein the width of the first dummy pattern is designed for less 1 μm where a concentration of solid content of the

SOG is around 5.2 wt%.

5. A semiconductor device as claimed in claim 1, further comprising,

a second dummy patter formed under the first dummy pattern; and

a fourth insulating layer formed directly on the substrate and on the second dummy layer, the fourth insulating layer having characteristics that its surface is planarized by a thermal treatment,

whereby the first dummy pattern is formed on the fourth insulating layer which is formed on the first dummy layer, and the circuit patterns are formed on the fourth insulating layer.

6. A semiconductor device as claimed in claim 5, wherein a shape and size of the second dummy pattern is almost the same as these of the first dummy pattern.

7. A semiconductor device as claimed in claim 5, wherein the fourth insulating layer is BPSG layer.

8. A semiconductor device as claimed in claim 5, wherein the second insulating layer is a SOG layer.

9. A semiconductor device as claimed in claim 6, wherein the widths of the first and second dummy patterns are fixed by a concentration of solid content of the SOG.

10. A semiconductor device as claimed in claim 6, wherein the widths of the first and second dummy patterns are designed for less 1 μm where a concentration of solid content of the SOG is around 5.2 wt%.

11. A semiconductor device as claimed in claim 1, further comprising,

a third dummy pattern formed between the first dummy pattern and the circuit area, the first insulating layer being not formed on the third dummy pattern.

12. A semiconductor device as claimed in claim 11, wherein a width of the third dummy pattern is almost the same as that of the first dummy pattern.

13. A semiconductor device as claimed in claim 11, wherein the distance between the first dummy pattern and the second dummy pattern is designed for over 0.9 μm.

14. A semiconductor device as claimed in claim 12, wherein the widths of the first and third dummy patterns are fixed by a concentration of solid content of the SOG.

15. A semiconductor device as claimed in claim 12, wherein widths of the first and third dummy patterns are designed for less 1 μm where a concentration of solid content of the SOG is around 5.2 wt%.

16. A semiconductor device as claimed in claim 1, further comprising,

a bonding pad formed on the semiconductor substrate in the circuit area;

a fourth dummy pattern surrounding the bonding pad, the first insulating layer being not formed on the fourth dummy pattern.

17. A semiconductor device as claimed in claim 16, wherein a width of the fourth dummy pattern is almost the same as that of the first dummy pattern.

18. A semiconductor device as claimed in claim 16, wherein a distance between the fourth dummy pattern and the bonding pad is designed for over 0.9 μm.

19. A semiconductor device as claimed in claim 17, wherein the widths of the first and fourth dummy patterns are fixed by a concentration of solid content of the SOG.

20. A semiconductor device as claimed in claim 117, wherein widths of the first and fourth dummy patterns are designed for less 1 μm where a concentration of solid content of the SOG is around 5.2 wt%.

21. A method for manufacturing a semiconductor device, comprising,

preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

forming a conductivity layer on the semiconductor substrate;

forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer;

forming a first insulating layer formed on an entire surface of the semiconductor substrate;

forming a second insulating layer formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns;

forming a third insulating layer formed on the exposed first insulating layer and the second insulating layer; and

removing the first, second and third insulating layers in the grid-line area.

22. A method for manufacturing a semiconductor device as claimed in claim 21, wherein the second insulating layer is formed by a SOG method.

23. A method for manufacturing a semiconductor device, comprising,

preparing a semiconductor substrate having a grid-line area and a chip area, the chip area having a circuit area and a dummy area surrounding the circuit area;

forming a conductivity layer on the semiconductor substrate;

forming circuit patterns in the circuit area and a dummy pattern encompassing the circuit area in the dummy area by etching the conductivity layer;

forming a first insulating layer formed on an entire surface of the semiconductor substrate;

forming a second insulating layer on the first insulating layer;

removing the second insulating layer which is formed on the first insulating layer on the dummy pattern until the surface of the first insulating layer is exposed;

forming a third insulating layer formed on the exposed first insulating layer and on the second insulating layer; and

removing the first, second and third insulating layers in the grid-line area.

24. A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is formed by a SOG method.

25. A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is removed by a RIE method.

26. A method for manufacturing a semiconductor device as claimed in claim 23, wherein the second insulating layer is a multi-SOG layer.